WHAT IS CLAIMED IS:

1. A solid state image sensor comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a pulse voltage to said storage region through said reset transistor,

wherein said drain regions of said plurality of amplifying unit pixels are connected to different drain lines row by row, and

said drain line is pulse driven to be set to a HIGH level potential at least during a period when said signal charge stored in said storage region is reset and a period when said signal charge stored in said storage region is detected.

2. The solid state image sensor of Claim 1,

wherein said drain line is set to a HIGH level

potential during a period when said read transistor is in an ON state.

3. The solid state image sensor of Claim 1, further comprising:

a vertical shift register for selecting one row of said plurality of amplifying unit pixels; and

a circuit for supplying, to said drain line on a corresponding row, a power pulse generated by using an output from one stage of said vertical shift register.

4. The solid state image sensor of Claim 1, further comprising:

a shift register for selecting one row or column of said plurality of amplifying unit pixels,

wherein each of said plurality of amplifying unit pixels is driven by a pulse used for driving said shift register.

5. The solid state image sensor of Claim 1,

wherein not less than two drain lines are set to a HIGH level potential during one blanking period for detecting signal charges of not less than two pixels adjacent to each other in a column direction out of said plurality of amplifying unit pixels.

6. The solid state image sensor of Claim 1,

wherein said drain line is set to a HIGH level potential during a period when said signal charge read from

said photoelectric conversion region is stored in said storage region and at least one period when said signal charge stored in said storage region is reset.

7. The solid state image sensor of Claim 1,

wherein said drain line is set to a HIGH level potential, for the purpose of removing unnecessary charge read from said photoelectric conversion region, during a period when said unnecessary charge is stored in said storage region and a period when said unnecessary charge stored in said storage region is reset.

8. The solid state image sensor of Claim 1,

wherein said drain line is set to a HIGH level potential, for the purpose of removing unnecessary charge read from said photoelectric conversion region to said storage region, during a period when both of said read transistor and said reset transistor are turned on.

9. The solid state image sensor of Claim 1,

wherein said drain line is made from the same interconnect layer as that used for forming gates of said read, detect and reset transistors.

10. The solid state image sensor of Claim 1,

wherein a line for connecting said storage region to a gate of said detect transistor is made from a first light blocking metal layer.

11. The solid state image sensor of Claim 1,

wherein said detect transistors of said plurality of amplifying unit pixels are connected to different signal lines column by column,

a line for connecting said storage region to a gate of said detect transistor and said drain line are made from a first metal layer, and

said signal line is made from a second metal layer above said first metal layer.

12. The solid state image sensor of Claim 1,

wherein said detect transistors of said plurality of unit pixels are connected to different signal lines column by column,

a line for connecting said storage region to a gate of said detect transistor and said signal line are made from a first metal layer, and

said drain line is made from a second metal layer above said first metal layer.